26.7 A Fully Integrated SoC for GSM/GPRS in 0.13µm CMOS

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Over more than a decade, cellular phones have made continuous progress in reducing component and chip count. The ultimate vision for years has been the single-chip CMOS transceiver. It promises lowest production cost, easiest board integration, and the highest flexibility in system optimization. However, crosstalk from digital into analog and RF blocks is a severe constraint. For cost reasons, a digital CMOS technology would be preferred [1, 2], but this makes RF design more complex and risky. To shorten the design cycle and minimize the risk, the SoC presented in this paper is based on mature RF and baseband chips, and is implemented in an RF-enhanced CMOS technology rather than a purely digital technology.

The SoC is the core component of a GSM phone. It integrates all digital, mixed-signal, and RF functionalities on a single CMOS die. Together with a PA module, a power-management IC, front-end switches, and filters, it makes up a complete quad-band GSM/GPRS system. The block diagram of the SoC is shown in Fig. 26.7.1.

The chip is implemented in a 0.13µm CMOS technology. It features linear MIM capacitors that can be placed on top of active regions, blocked polysilicon resistors, high ohmic substrate for crosstalk reduction and improved inductor Q-factor, and up to 6 metal layers with a thicker top layer. Gate-oxide thickness is 2.2nm for the core device and 5.2nm for the 2.5V analog and I/O-device. The core device has 100MHz f_T and 60GHz f_{max}. For optimized performance, both device types are selectively used in the RF blocks.

The digital part comprises a microcontroller, a DSP, 256kB SRAM, 2Mb ROM, and several interfaces. The DSP delivers 104 MIPS for modem functionality and voice coding. The microcontroller, running at 52MHz, supports the protocol stack (GSM and GPRS), MMI, and JAVA functionality. Seventeen different power domains are used to minimize power consumption and crosstalk. The nominal supply voltage is 1.5V. A page-mode control and various interface standards are supported.

Four ADCs and two DACs are implemented for receive, audio, and control functions. The supply voltage for all mixed-signal blocks is 2.5V. In the receive part, a 14b ΔΣ ADC with a SC single-bit 2-2 MASH architecture, clocked at 26MHz, is used. It requires only a 3rd-order baseband pre-filter. The ADC achieves 89dB SNR over 100kHz bandwidth and PSRR of better than 60dB while drawing 5.6mA.

The transmitter features direct modulation with a ΔΣ fractional-n PLL, thus no TX-DAC is required. An 11b DAC allows tight control of the PA power level and ramp-up and ramp-down slopes. The DAC core is an 8b resistor string. Interpolation is used to achieve 11b resolution. The DAC output buffer supplies up to 5mA into the PA control input.

The audio section consists of microphone supply, input amplifier, ADC, DAC, and two differential output amplifiers. The audio ADC is a 2nd-order single-bit SC ΔΣ modulator, preceded by a Class-A LNA with programmable gain from 0 to 24dB. SNR over the 20kHz audio band is > 80dB for all gain settings. The audio DAC achieves 13b resolution from an 8b R-string core. It occupies 0.1mm^2 and draws 1mA. In a single-chip implementation high PSRR of the mixed-signal blocks is a must. Class-D amplifiers are known for good efficiency but also low PSRR. Therefore, three-stage class-AB amplifiers with nested Miller compensation are used instead to deliver MP3 quality signals with up to 200mW into 16Ω earpieces and up to 10nF parallel load capacitance. The whole audio transmit path achieves SNR>80dB, THD<0.1%, and PSRR>60dB over 20kHz bandwidth. The amplifier gain can be programmed in 3dB steps over an 18dB range.

The RF transceiver part (Fig. 26.7.2) is based on the architecture presented in [3], but the receive filter is now fully integrated and the layout is optimized. A zero-IF approach in RX and a direct-modulation concept in TX path are used.

The ΔΣ modulation approach in TX is chosen because of its robustness against process variations. The limited PLL loop bandwidth is compensated for by predistortion of the modulation signal. The semi-digital VCO uses a SC bank for coarse frequency adjustment and MOS varactors for fine tuning. It runs at twice the carrier frequency for the upper bands and at four times the carrier frequency for the lower bands. The PLL loop filter is optimized for high suppression of the ΔΣ quantization noise especially around the 400kHz offset. A critical parameter in GSM is TX leakage into the RX bands. Figure 26.7.3 shows the TX spectrum in the 900MHz RX band with a 903.2MHz transmit frequency. Only two out of five permissible exceptions occur. The output power from the PA driver is above 1.5dBm in all bands, leaving enough margins for board losses. Figure 26.7.4 shows the TX modulation spectrum at the 1872.2MHz center frequency, which is close to 1872MHz, a multiple of all digital frequencies.

The zero-IF architecture in RX is chosen because of its superior blocking performance and low sensitivity against spurs in the LO signal. A noise optimized LNA and a mixer with a hard switching LO signal result in an overall NF of 3dB. The receiver sensitivity in a typical GSM application, including the matching network, is measured as -111dBm (Class II RBER, without fading). An AM suppression of better than 87dB is achieved by isolating the LNA from the LO and by extremely symmetrical layout. The high-resolution ADC (14b) reduces the effort for gain control and pre-filter, while saving the die area and lowering the power dissipation.

Crosstalk from the digital blocks into RF is one of the biggest concerns in single-chip transceivers. A critical coupling path is shown in Figure 26.7.6. Substrate noise pickup, package crosstalk, magnetic coupling between the coils, and supply coupling degrade the RF performance. High-frequency harmonics of the system clocks near the LO frequency couple into the VCO and generate spurs in the TX modulation spectrum. Low-frequency components of the system clocks couple into the LO path and generate spurs in the corresponding RX band. These effects are reduced by proper placement of on-chip blocking capacitances. Key RF measurement results are summarized in Fig. 27.6.7.

A fully integrated SoC for quad-band GSM and GPRS is presented. The achieved crosstalk performance is the main factor for successful integration. No special process options (such as triple well, deep trench, etc.) are used or required for crosstalk reduction. This chip fulfills all the GSM and GPRS specifications at reduced cost, area, and power consumption compared to common two-chip implementations.

Acknowledgements:
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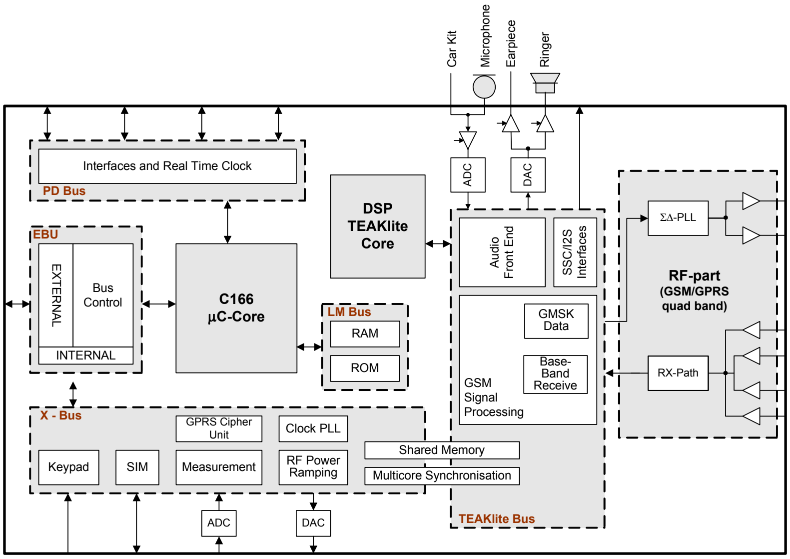

Figure 26.7.1: Block diagram of the SoC.

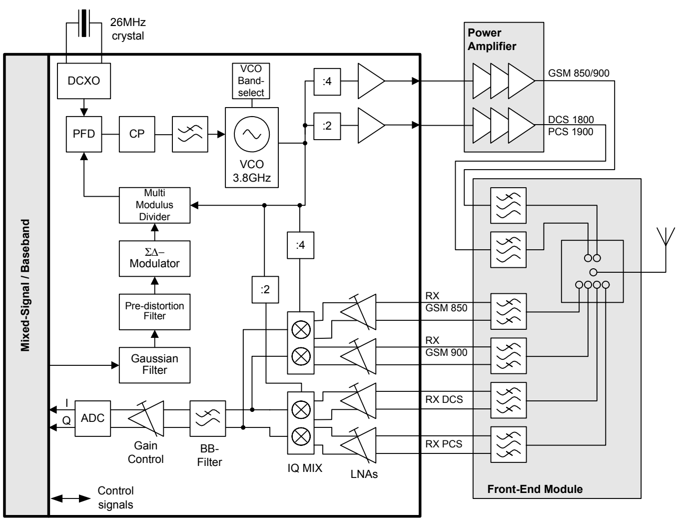

Figure 27.6.2: Detailed block diagram of RF and analog baseband sections.

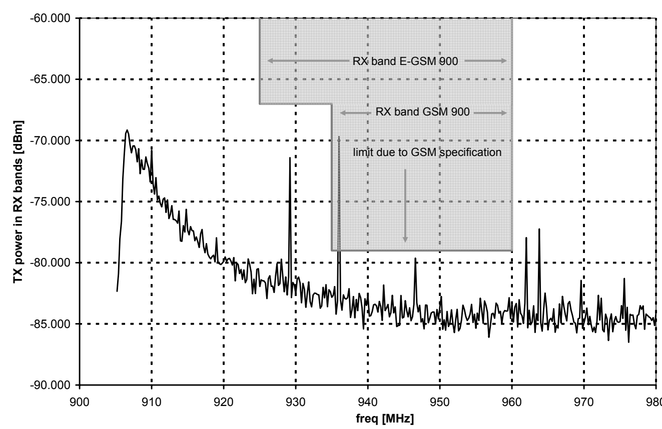

Figure 26.7.3: Measured TX spectrum in the 900MHz RX band with 903.2MHz transmit frequency.

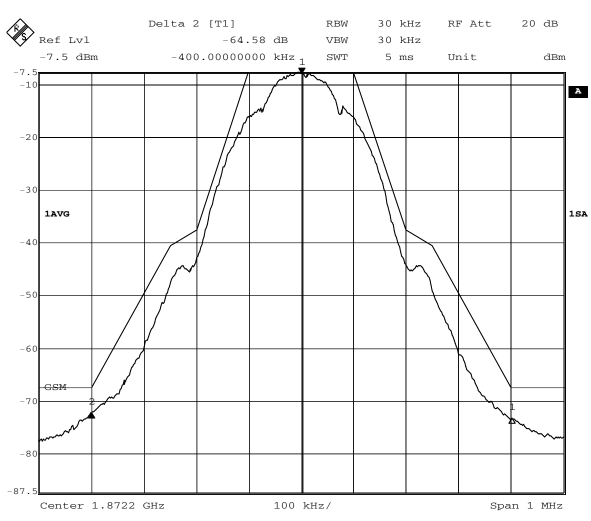

Figure 26.7.4: Measured TX spectrum at 1872,2MHz center frequency.

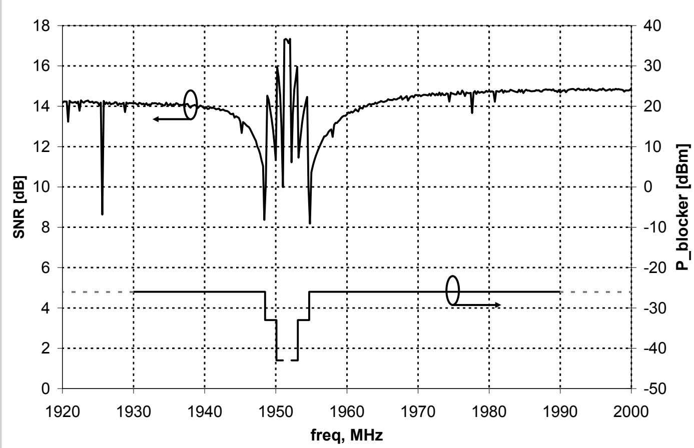

Figure 26.7.5: Measured blocking performance (as SNR equivalent) at 1951.6MHz center frequency.

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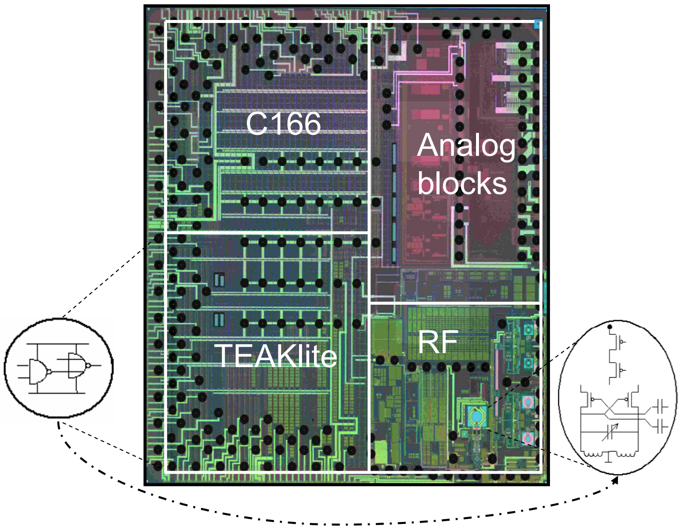

Figure 26.7.6: Chip micrograph and crosstalk situation.

	GSM800/900	DCS1800/PCS1900
Sensitivity RX, dBm	-112.5	-110.5
Noise figure, dB	2.6	3.1
AM-suppression, dB	>90	>87
I-Q-phase error, deg	<1.0	<1.8
Gain variation, dB	0.6	0.6
Flicker noise corner frequency, kHz	0.55	1.75
Phase noise @400kHz, dBc/Hz	-127.8	-120.6
Phase noise @20MHz, dBc/Hz	-164.2	-158.2
Output power, dBm	3.2	3

Figure 26.7.7: Key RF measured data.